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A LOW NOISE AlGaAs/GaAs FET WITH P+-GATE AND SELECTIVELY DOPED STRUCTURE

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Abstract

A low noise AlGaAs/GaAs FET with p^+-gate and selectively doped structure has been developed. The FET utilizing a two dimensional electron gas has a closely spaced electrode planar structure on an MBE wafer. A 0.5 μm gate FET exhibited marked room temperature performances of 310 mS/mm transconductance and 1.2 dB noise figure with 11.7 dB associated gain at 12 GHz.

Introduction

Field effect transistors based on an N-AlGaAs/GaAs selectively doped structure have recently attracted much attention for applications to high speed ICs. Those FETs are also attractive for low noise microwave devices due to high electron mobility of the two dimensional electron gas (2DEG) in the selectively doped structure [1],[2]. A 1.4 dB noise figure at 12 GHz was reported for such FETs [2]. The FETs with the selectively doped structure reported previously usually have a recessed gate structure [2]-[4]. A surface n^+-GaAs layer was used outside the gate for accumulating as much two dimensional electron gas (2DEG) density as possible and making ohmic contact formation easy. However, this structure requires precise etching of the recessed region and possibly increases the gate fringing capacitance.

In this work, a new low noise FET, based on the N-AlGaAs/GaAs selectively doped structure, has been developed. The FET has a planar p^+-gate structure with small source resistance. A 0.5 μm-gate device exhibited marked room temperature performance of 1.2 dB noise figure with 11.7 dB associated gain at 12 GHz.

Device Structure

The structure of the newly developed FET is shown in Fig. 1. The gate is made with an Al electrode and an interposed highly doped p-type GaAs thin layer on n-type layers for 2 DEG formation. Energy band diagrams at the gate and between the gate and the source are shown in Figs. 2(a) and (b), respectively. The surface potential of the n-type layers at the gate is raised by the p^+-layer compared to that outside the gate, if the acceptor density of the p^+-layer is much higher than the donor density of the n-type layers. This enables using a thicker and/or more highly doped n-layer than that used in conventional FETs with Schottky barrier gates. Therefore, much accumulation of 2 DEG and small source resistance can be attained without gate recessing. The p^+ -GaAs layer is so highly doped and thin that a planar gate structure and small gate resistance can also be realized. Furthermore, the gate has a large potential barrier due to the p-n junction, so that high reliability for the gate electrode can be expected.

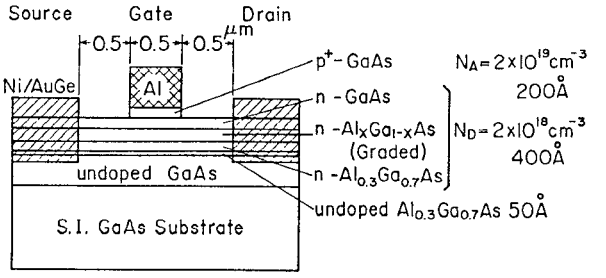

Fig. 1 Structure of the developed FET.

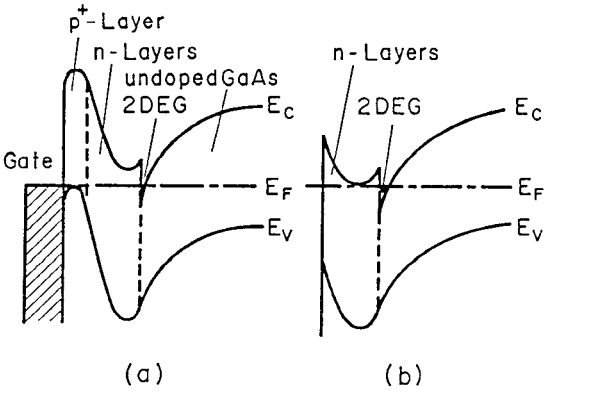

Fig. 2 Energy band diagram in thermal equilibrium. (a) At the gate. (b) Outside the gate.

Other important features of the new FET shown in Fig. 1 are also related to technologies for source resistance reduction. An n-GaAs layer is used for the top layer of the n-type layers so as to make ohmic contact formation and surface protection easy. 2 DEG sheet density is limited to a relatively small value of about 1×10^{12} cm^{-2}, so that a close space structure between the source and the gate [5] is employed in order to reduce the 2 DEG layer resistance at room temperature. The gate length and the spacing between the gate and the source were designed to be 0.5 μm. Devices with four gate widths, 100 μm, 140 μm, 200 μm and 280 μm were examined. The unit gate width is 50 μm for 100 μm and 200 μm devices, and 70 μm for 140 μm and 280 μm devices. 200 μm and 280 μm devices have two gate pads.

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Consequently, advantages of this new structure are a planar gate structure with small gate fringing capacitance, small parasitic resistances, high reliability for the gate electrode and an easy fabrication process, as described in the following.

Device Fabrication

Fabrication steps for the developed FET are shown in Fig. 3. p^+-GaAs(200 Å)/n-GaAs(100 Å)/n-$Al_xGa_{1-x}As$ (graded composition) (200 Å) / n-$Al_{0.3}Ga_{0.7}As$ (100 Å) /undoped $Al_{0.3}Ga_{0.7}As$(Spacer)(50 Å)/undoped GaAs(1 μm) layers were grown by molecular beam epitaxy (MBE) on a semi-insulating GaAs substrate: -(1). The p^+-GaAs layer was Be doped with 2×10^{19} cm^{-3} and n-type layers were Si doped with 2×10^{18} cm^{-3}. The mobilities of 2 DEG were 6500 cm^2/Vs at room temperature and 89000 cm^2/Vs at 77 K. A 0.5 μm long and 0.4 μm thick gate electrode was made with Al by side-etching technique using a photoresist mask for source and drain contacts: -(2). Ni/Au-Ge ohmic metal layers were evaporated through the photoresist mask: -(3). After the lift-off process, the Ni/Au-Ge layers were alloyed with those semiconductor layers forming source and drain ohmic contacts, so that the source and drain contacts can be formed in the self-alignment process with the gate electrode: -(4). Then, the p^+ -layer outside the gate was etched using the gate, source and drain electrodes as etching masks: -(5). This p^+-layer etching is the only step in addition to the conventional fabrication process for planar Schottky barrier gate GaAs FETs [5]. Therefore, the fabrication process is simple and it is easy to form short gate electrodes. Figure 4 shows a cross sectional view of a fabricated 0.5 μm gate FET.

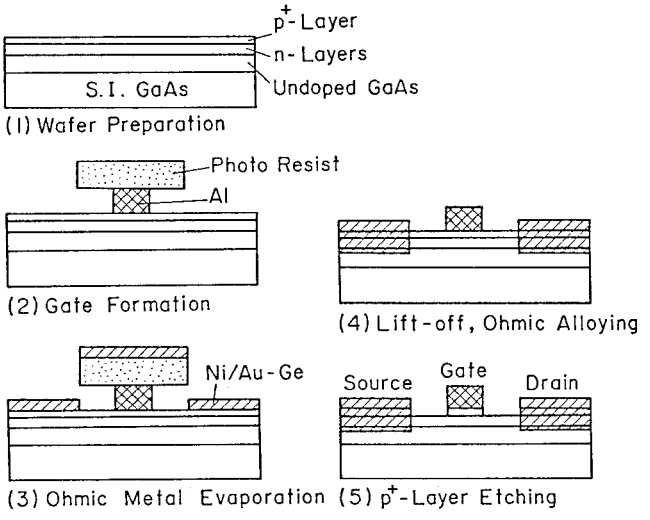

Fig. 3 Fabrication steps for the developed FET.

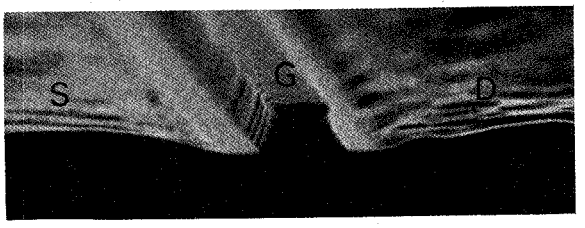

Fig. 4 Cross sectional view of a 0.5 μm gate FET.

Performance

The developed AlGaAs/GaAs selectively-doped-structure FET with a p^+-gate exhibited high DC and RF performances. Figure 5 shows static characteristics of a FET with a 0.5 μm long and 200 μm wide gate at room temperature. These characteristics show low saturation voltage and markedly high transconductance due to small source resistance. The maximum transconductance was 62 mS, that is 310 mS/mm gate width. The FET also exhibited enhanced transconductance of 90 mS (450 mS/mm) at 77 K. The source resistance is estimated to be 3.5 Ω at room temperature which is the sum of the contact resistance of 1 Ω and the resistance of the 2 DEG layer between the source and the gate of 2.5 Ω for 200 μm gate width. This value, that is 0.7 Ω mm, is relatively small, compared to FETs based on N-AlGaAs/GaAs selectively doped structure reported so far [1]-[4]. The drain conductance was about 15 mS/mm.

Figure 6 shows s-parameters from 2 to 12 GHz for a FET with 200 μm gate width (50 μm x 4). The magnitude of S_{21} is fairly large, corresponding to high

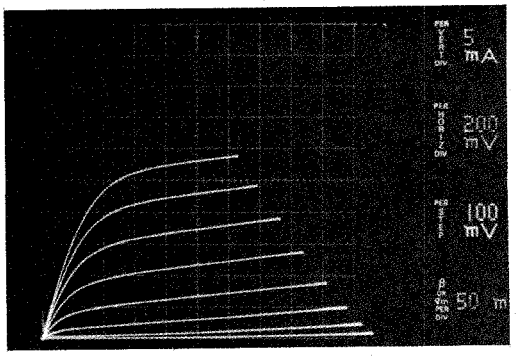

Fig. 5 Drain I-V characteristics of a 0.5 μm gate FET. Gate width is 200 μm. H:0.2 V/div, V:5 mA/div, Gate:-0.1 V/step.

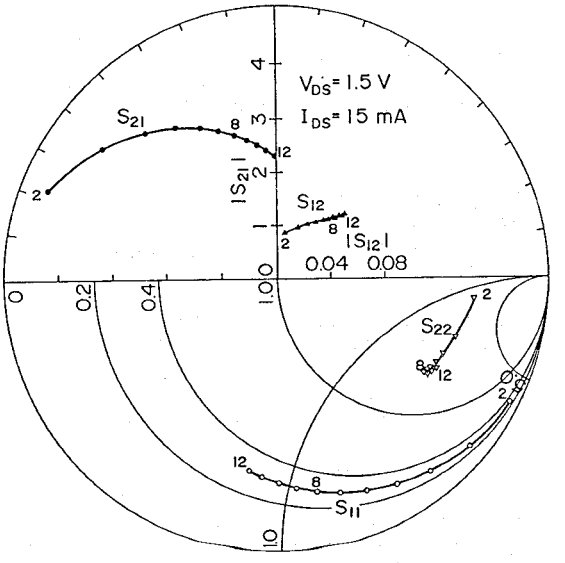

Fig. 6 S-parameters of the developed FET. Gate width is 200 μm.

transconductance. The phase rotation of S_{11} and the magnitude of S_{12} are both small. This indicates small gate capacitance and small drain gate feedback capacitance, in spite of using highly doped n-type layers. This is possibly due to small gate fringing capacitance of the planar gate structure.

The noise performance of the new FET was evaluated in the packaged form at room temperature. The FET exhibited marked noise performance as shown in Figs.7 and 8. Figure 7 shows drain current dependences of minimum noise figure NFmin and associated power gain Ga at 12 GHz for an FET with a 200 μm wide gate. Marked low noise and high gain performance was obtained, even at low drain current level. Figure 8 shows gate width dependence of the noise performance at 12 GHz. Zu represents the unit gate width. The best results were obtained at around 200 μm gate width. Room temperature performance values for 0.5 μm gate FETs were 0.34 dB noise figure with 14.8 dB associated gain and 1.2 dB noise figure with 11.7 dB associated gain at 4 GHz and 12 GHz, respectively.

Table I shows a summary of device parameters and performance for the FET with a 200 μm wide gate. Noise performances are comparable to the best data for quarter micron gate GaAs MESFETs. However, parasitic resistances and drain conductance g_d are fairly large as yet, compared to refined GaAs MESFETs. Further optimization of the device design including crystals will possibly push the noise performance improvement.

Conclusion

A new low noise FET, based on the N-AlGaAs/GaAs selectively doped structure, has been developed. The FET has a planar structure with a p^+-gate and a close space structure between the gate and the source in order to have small source resistance. A 0.5 μm gate FET exhibited marked room temperature performances of 310 mS/mm transconductance , 0.34 dB noise figure with 14.8 dB associated gain at 4 GHz, and 1.2 dB noise figure with 11.7 dB associated gain at 12 GHz.

Acknowledgment

The authors wish to thank Drs. N Kawamura and Y. Takayama for their helpful suggestions and encouragements. They also thank Drs. T. Itoh, H. Terao and H. Watanabe for their valuable discussions, and Y. Ara and Y. Fujiki for microwave measurements.

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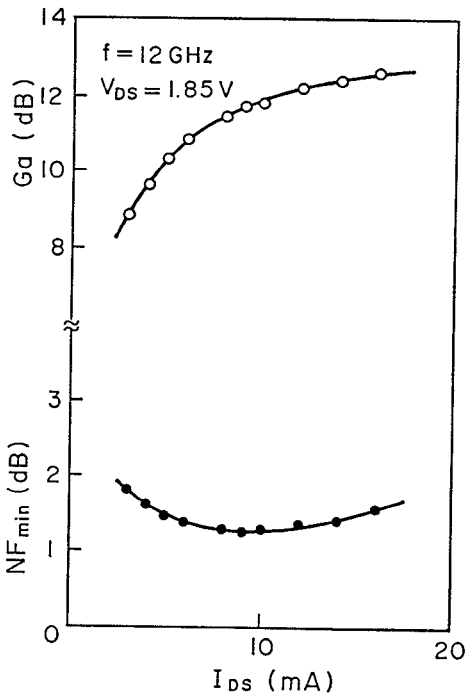

Fig. 7 Drain current dependences of minimum noise figure NFmin and accociated gain Ga.

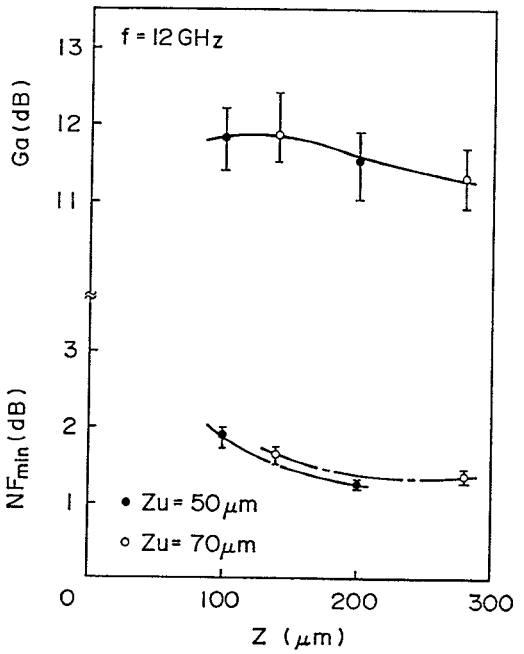

Fig. 8 Gate width dependence of noise performance.

Table I Summary of device performance for a 0.5 μm long, 200 μm wide FET.

R_s (Ω)	R_g (Ω)	g_m (I_d=10mA) (mS)	g_d (I_d=10mA) (mS)	V_p (V)	NF (Ga) 4 GHz (dB)	NF (Ga) 12 GHz (dB)
3.5	0.9	50	3.0	-0.7~ -1.4	0.34 (14.8)	1.2 (11.7)